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One to three 50-minute sessions. Suitable for sixth through twelfth grades. Each

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- Lecture with slides and handout covering implementation of a full adder as a “chip” or digital Works macro. (10 minutes)
- Exercise: Implement a five bit ripple-carry adder using the trainer software/hardware and validate that it computes sums of binary digits. (15 minutes)
- Lecture: Combinational and sequential circuits. (10 minutes)
- Exercise: Implement an S-R latch and, time permitting, extend it to a D-latch. (15 minutes)

Students who complete this session successfully will be able to:

- Compare half and full adders with respect to function.
- Explain the operation of a ripple-carry adder.
- Describe the fundamental limitation of a ripple-carry adder for the addition of large (*e.g.* 32-bit) numbers.
- Explain what a nanosecond is.

Module 3 shows students how to derive a Boolean expression from a “word problem” and how to implement the expression in digital logic.

Completion of Module 1 or similar knowledge, and experience with the chosen tool.

- Lecture: Introduction of Kat’s Cat Checker, the problem. (10 minutes)
- Exercise: Cat checker (E  V  Explain wha impleme(61 0.004 55Td)-10(ag)]TMC i0 Td10(a:x)-10(I)25(-